Everywhere Digital-Assisted High-Performance Analog-to-Digital Converter

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Outline

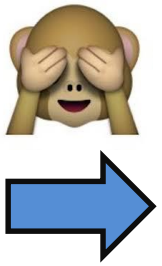
- ❑ Motivations
- ❑ Design Examples
- ❑ Conclusion

About Calibration

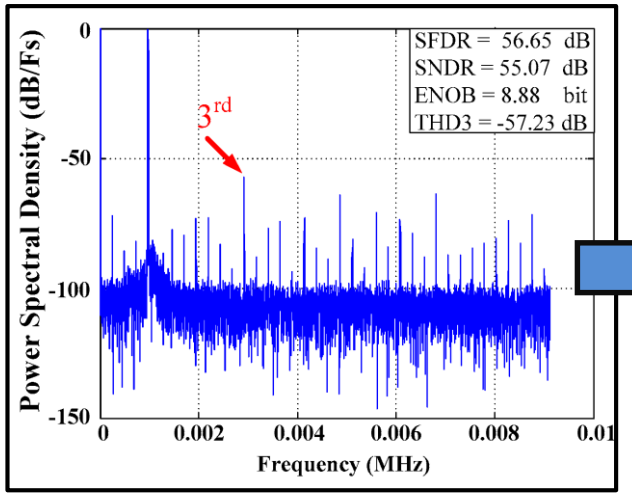
Engineering:
Calibration

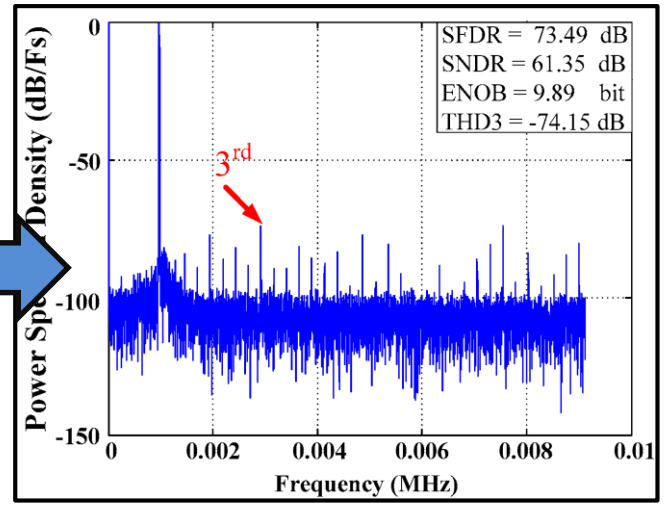
In daily life (depend on the level) :
化妝　　喬裝

Before Lite Calibration



After Lite Calibration





About Calibration

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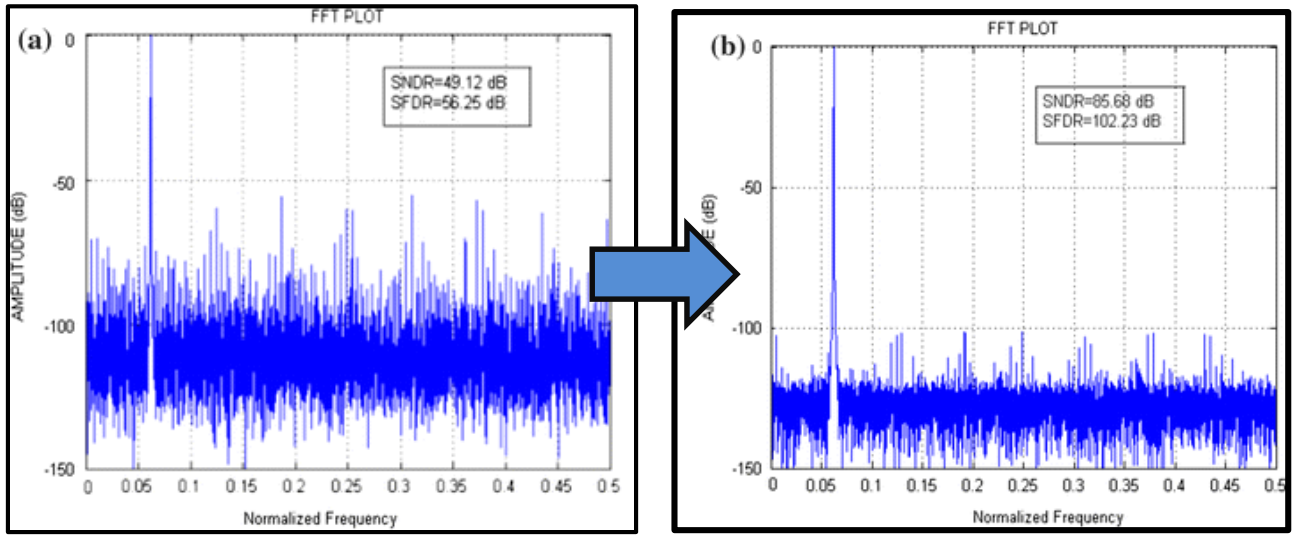
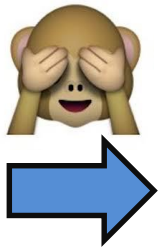


Before Heavy Calibration



After Heavy Calibration

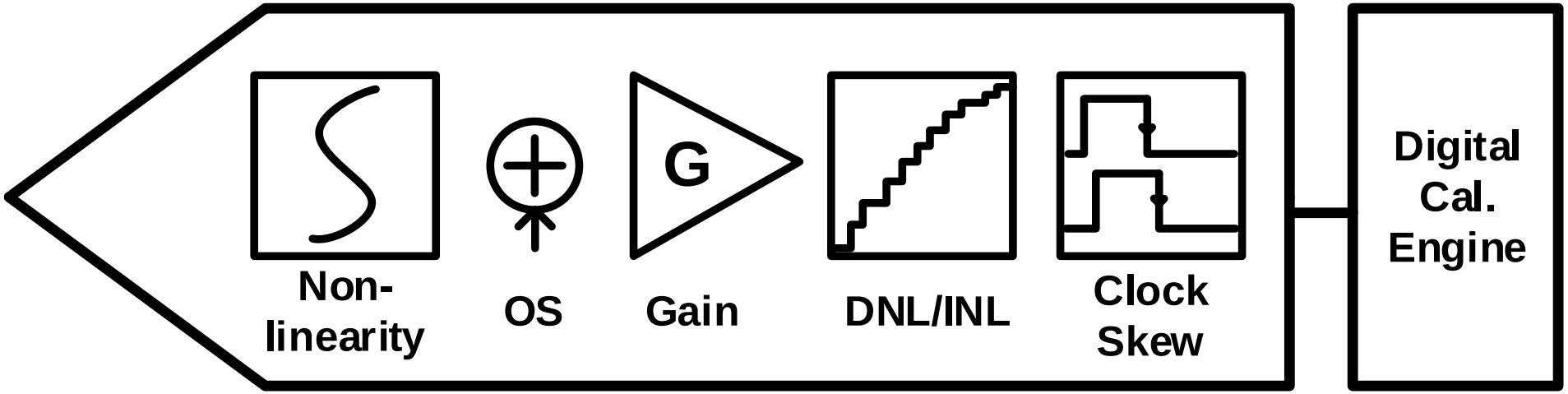
Digital-Assisted A/D

Digital-Assisted Solution:

- Effective for most of error in ADC
- Technology scaling friendly
- Preserve ADC integrity

Categorized in:

- Background
- Foreground

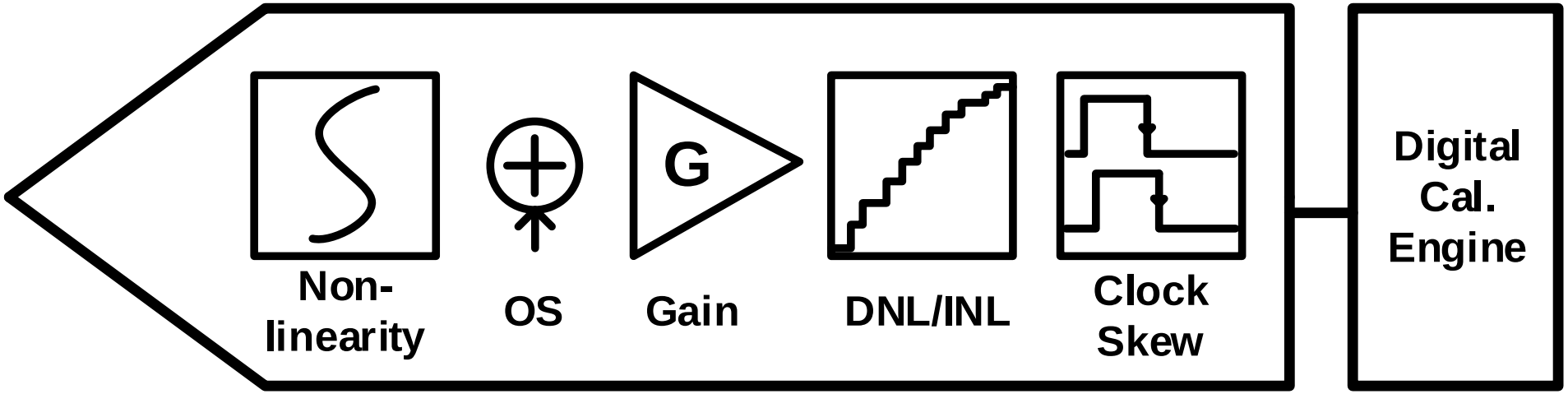


- With digital or analog /FB correction, sometime with analog-assisted

Digital-Assisted A/D

Considerations:

- Cost, including area, power, complexity and convergence
- Analog overhead (Auxiliary Channel, Additional DAC, etc.)
- Input constraints and others limitation on ADC (Loss DR, etc.)



- Need to consider calibration efficiency, necessity and testing

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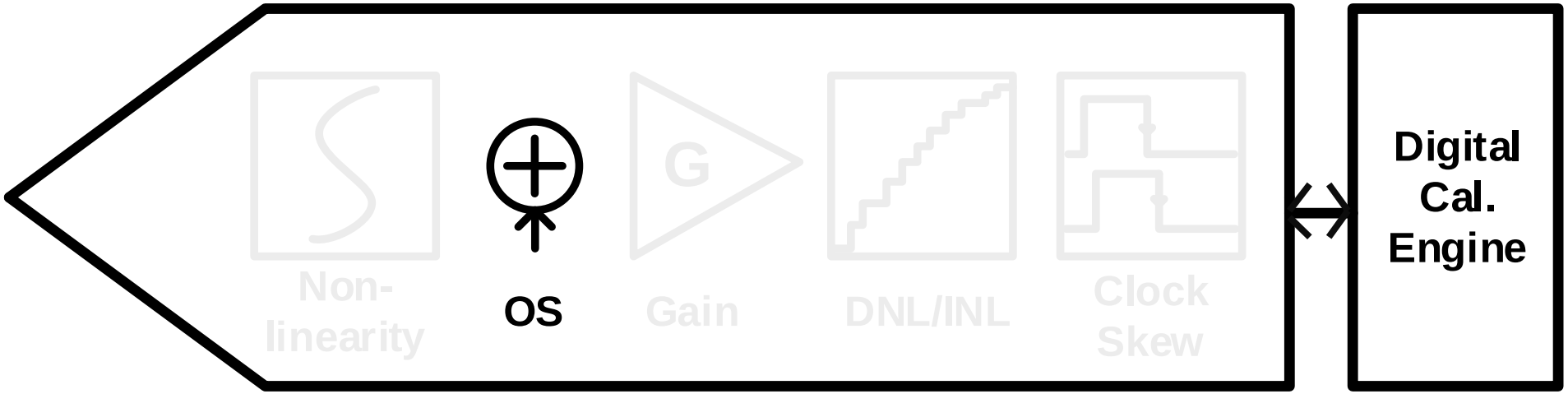
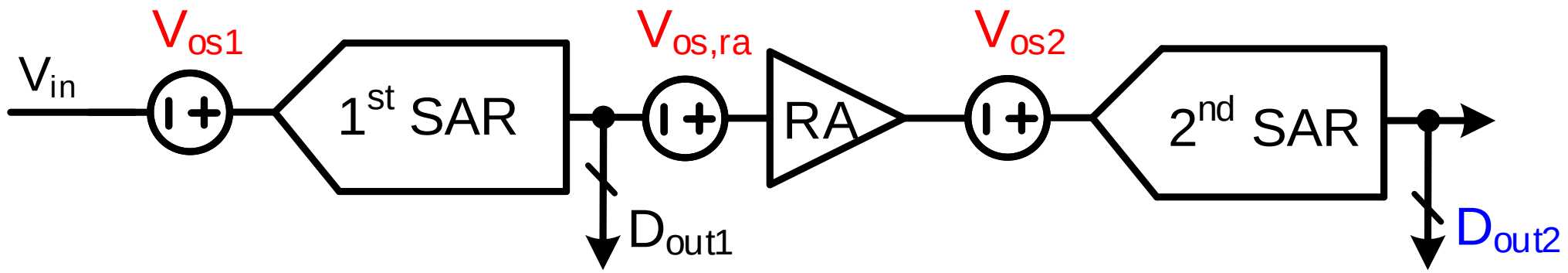
- ❑ **Design Examples**
- ❑ Conclusion



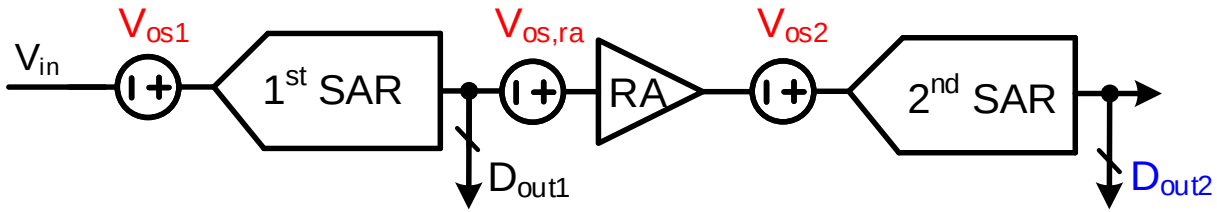
SAR-Assisted Pipeline ADC with Background Offset Calibration

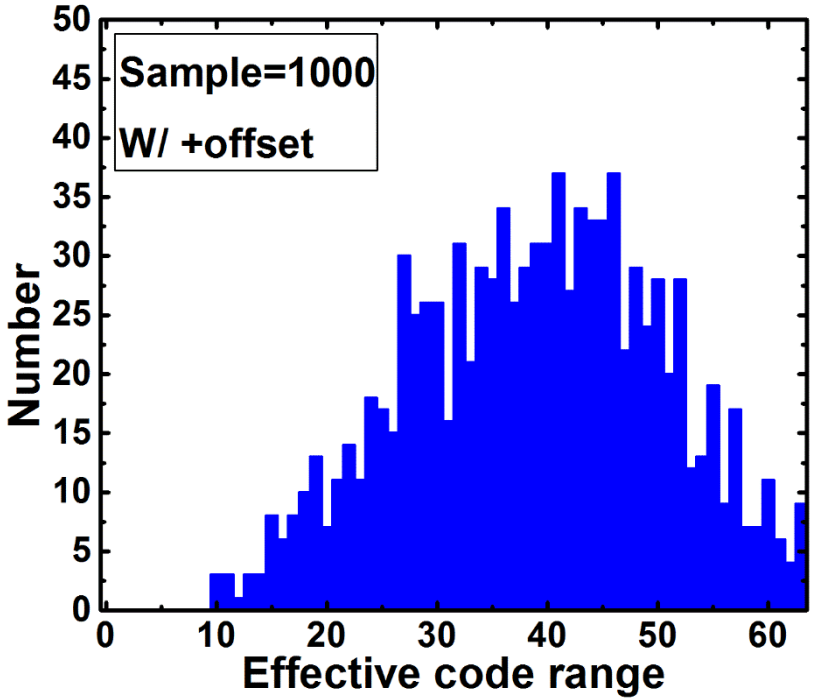
Offset in Pipeline-SAR ADCs

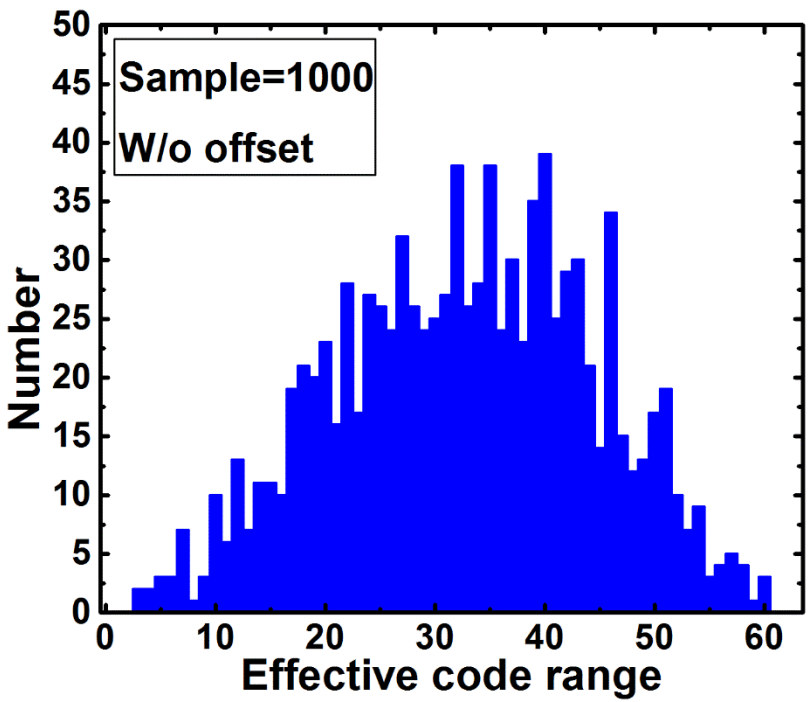


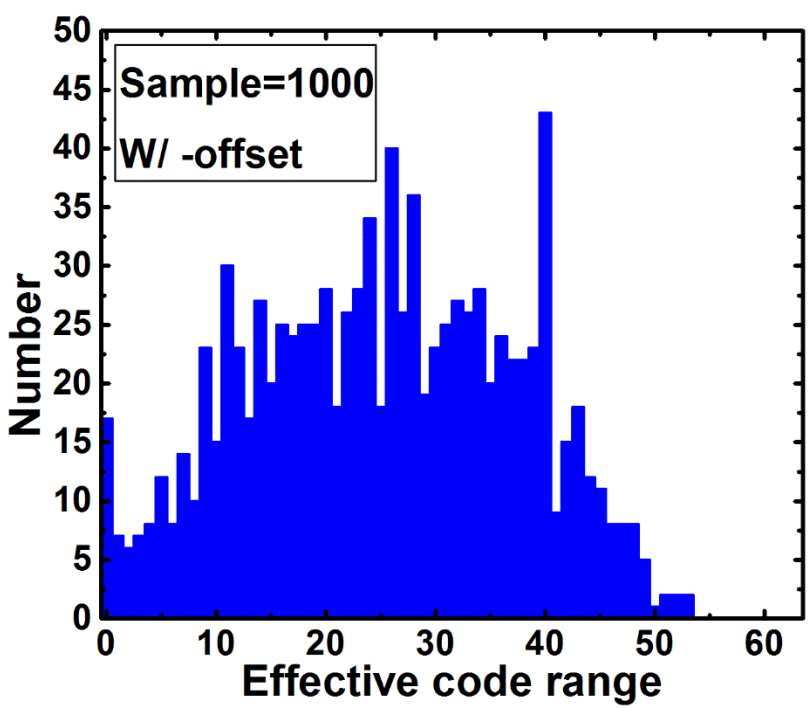
- **Offset mismatch between 2 stages from:**
  - V_{os1} : First stage SAR
  - $V_{os,ra}$: Residue amplifier
  - V_{os2}: Second stage SAR
- **Can saturate the second stage input, must handle with analog feedback**

Second Stage Code Histogram



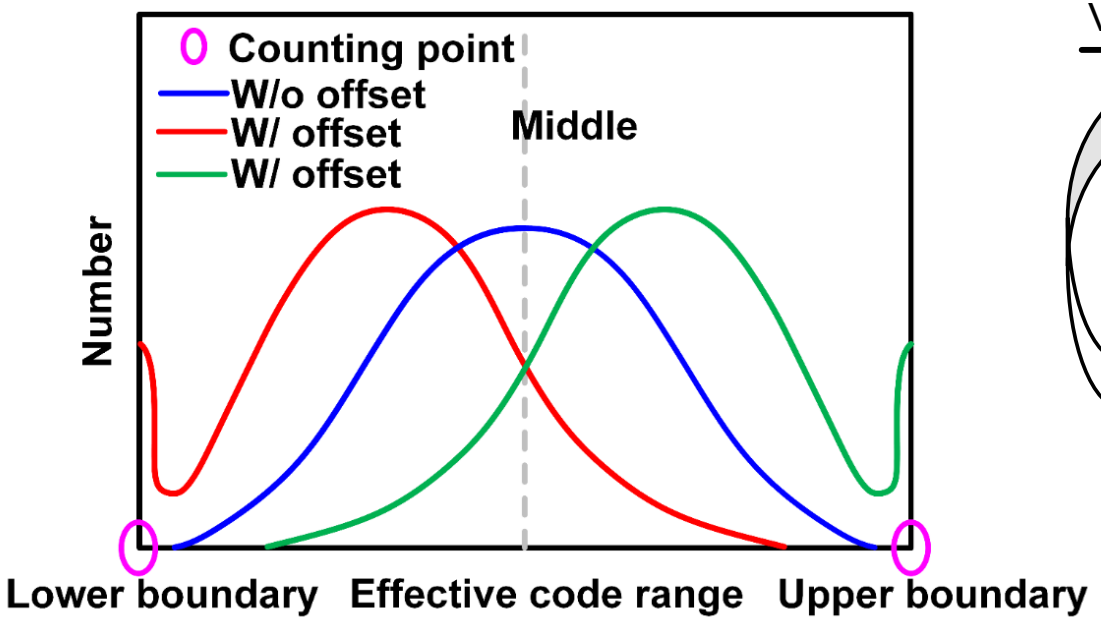


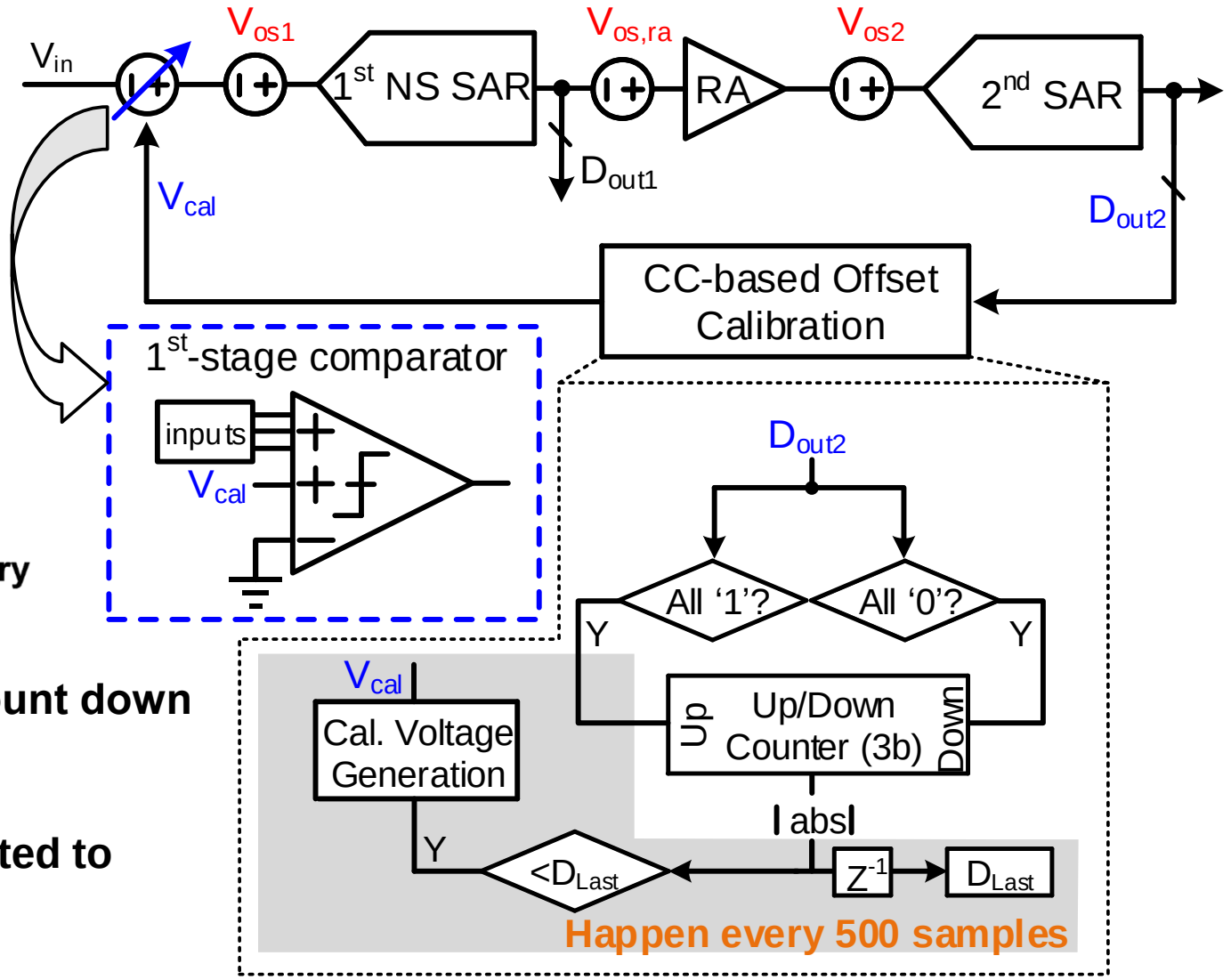




- Code range is confined with the effective range when the offset is 0
- Code range varies with offset
- Code saturates by one side because of offset

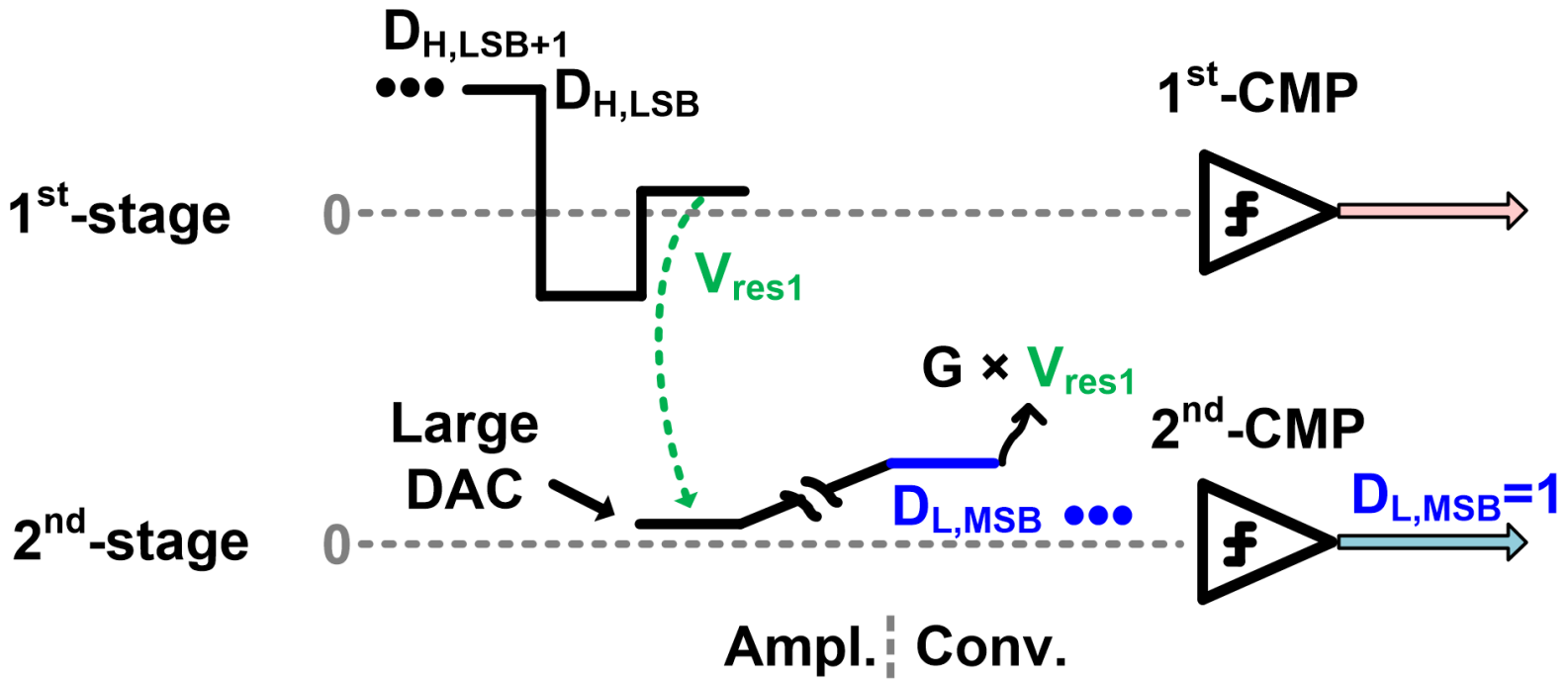
Inter-stage Offset Calibration Scheme (1)





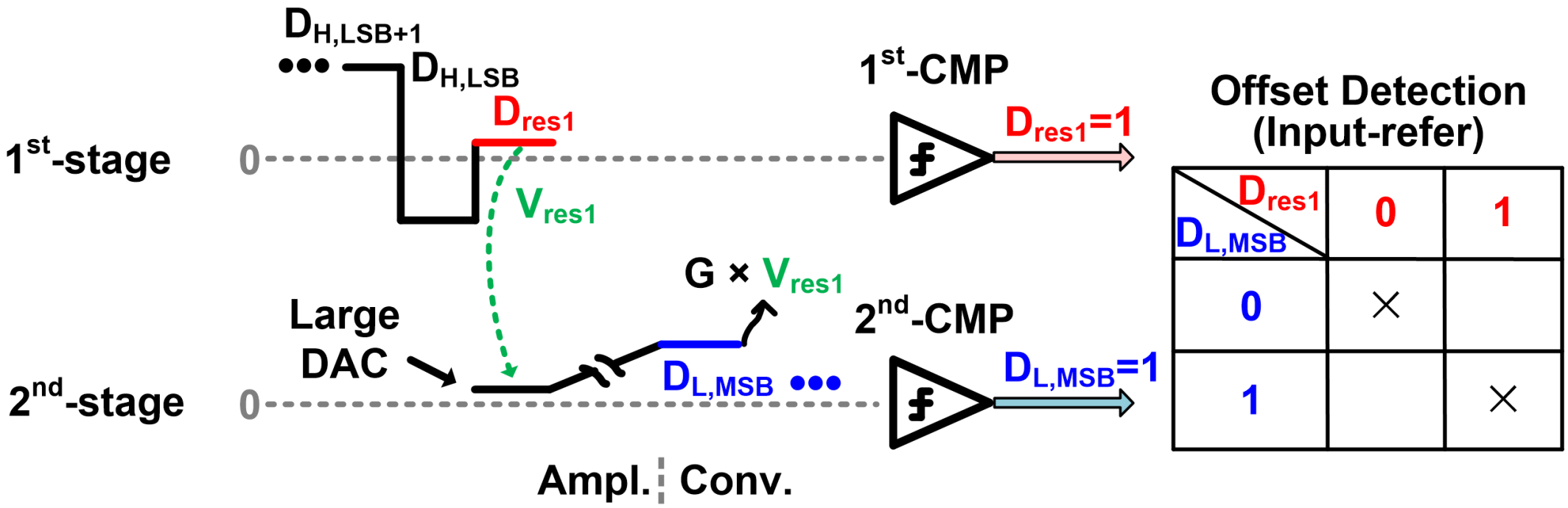
- **D_{out2} equals to all '1', count up, vice versa count down**
- **The offset is calibrated on chip**
- **Convergence speed and accuracy are weighted to chose N**

Inter-stage Offset Calibration Scheme (2)



- No comparison needed for V_{res1} in conventional pipeline operation
- Sign of V_{res1} not change after amplification **(Utilize this redundancy?)**

Comparison of MASH 0-N and MASH N-0

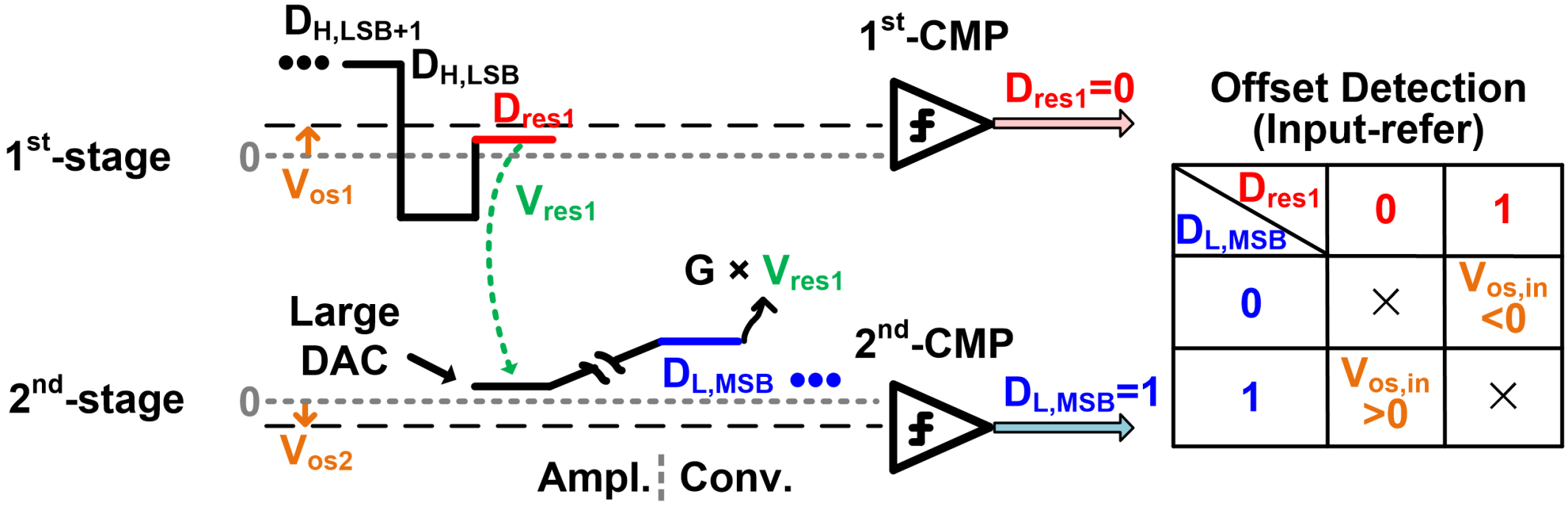


Offset Detection (Input-refer)

$D_{L,MSB}$ \ D_{res1}	0	1
0	×	
1		×

- 1st-stage redundant comparation detects the sign of V_{res1}
- D_{res1} & $D_{L,MSB}$ should <u>be the same without offset</u>

Amplify Residue to the Next Stage



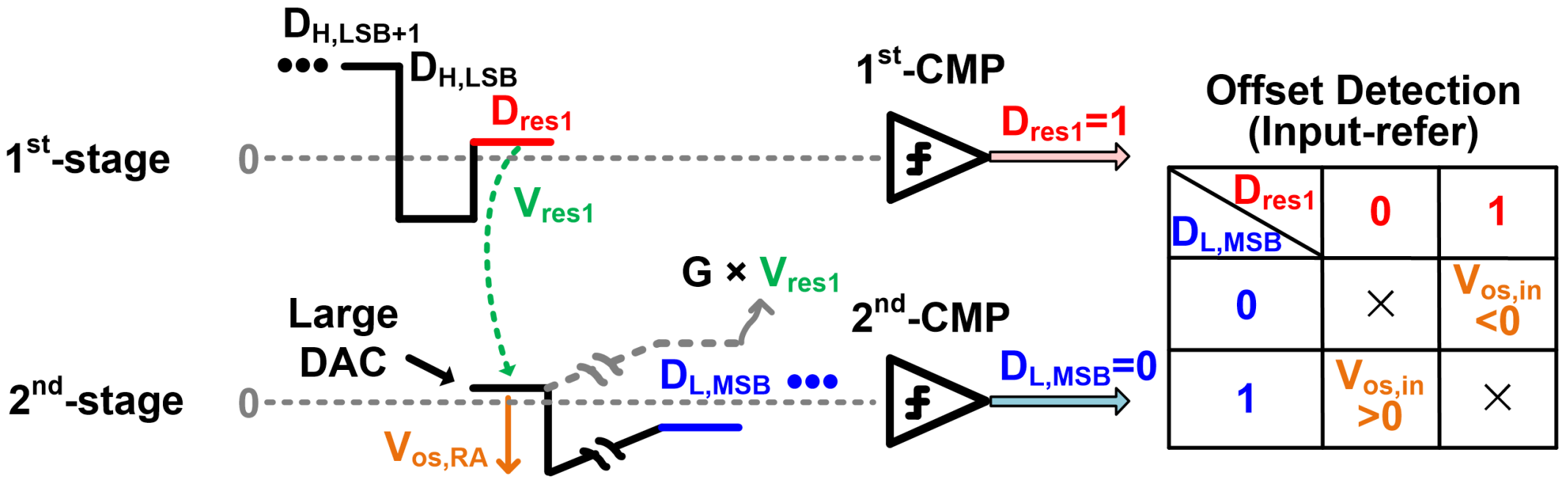
Offset Detection (Input-refer)

$D_{L,MSB}$ \ D_{res1}	0	1
0	×	$V_{os,in}$ <0
1	$V_{os,in}$ >0	×

- **Detecting the sign of overall offset voltage ($V_{os,in}$)**

$$V_{os,in} = V_{os1} - \frac{1}{G} V_{os2}$$

Simplified ADC Schematic

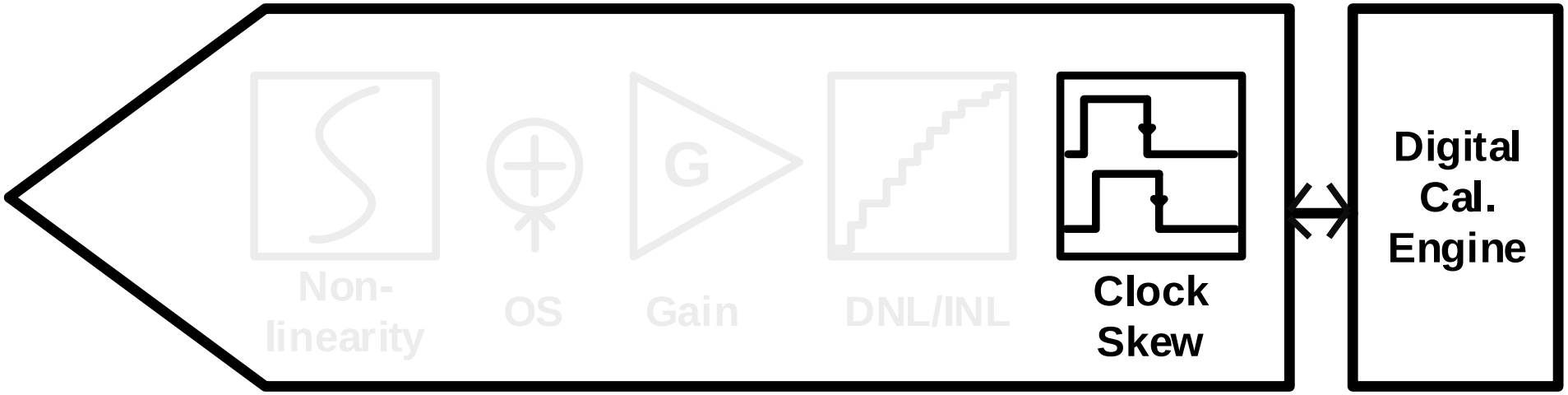


Offset Detection (Input-refer)

$D_{L,MSB}$ \ D_{res1}	0	1
0	×	$V_{os,in}$ <0
1	$V_{os,in}$ >0	×

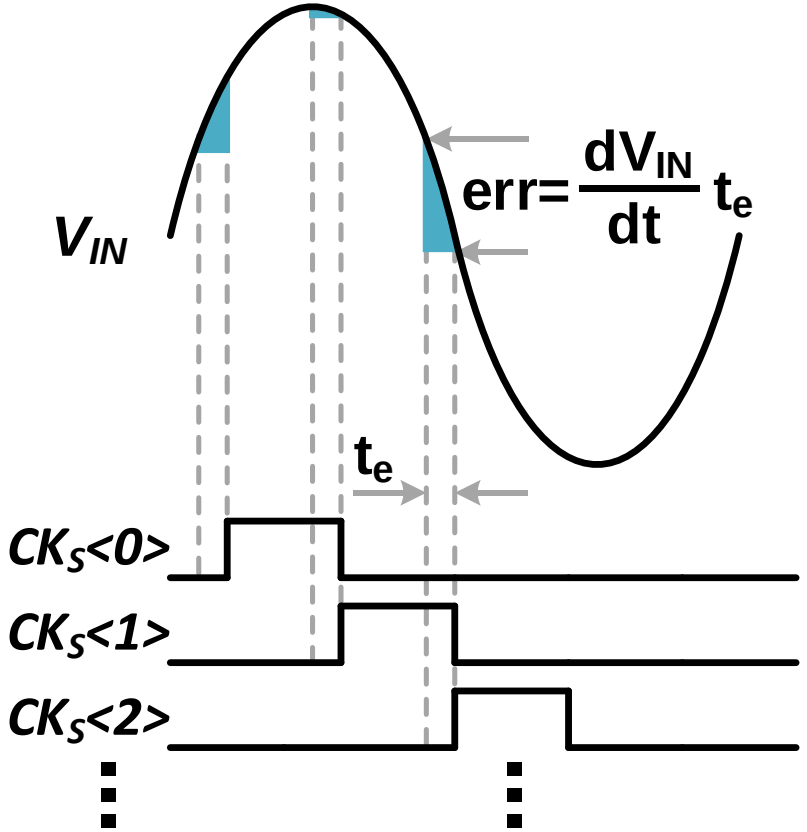
- **Same criteria for RA's offset detection**

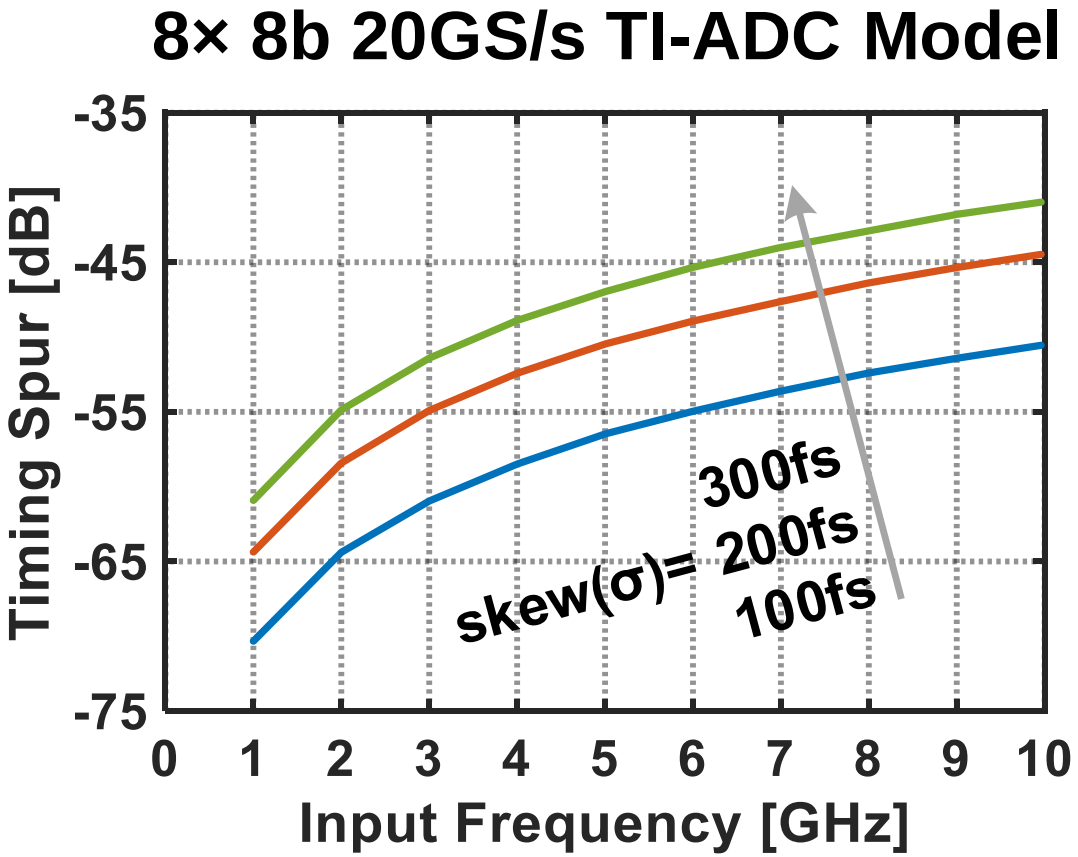
$$V_{os,in} = V_{os1} - \frac{1}{G} V_{os2} + \frac{1}{G} V_{os,RA}$$



A 20GS/s 8b Time-Interleaved Time Domain ADC with Input-Independent Background Timing Skew Calibration

Timing Skew Mismatch





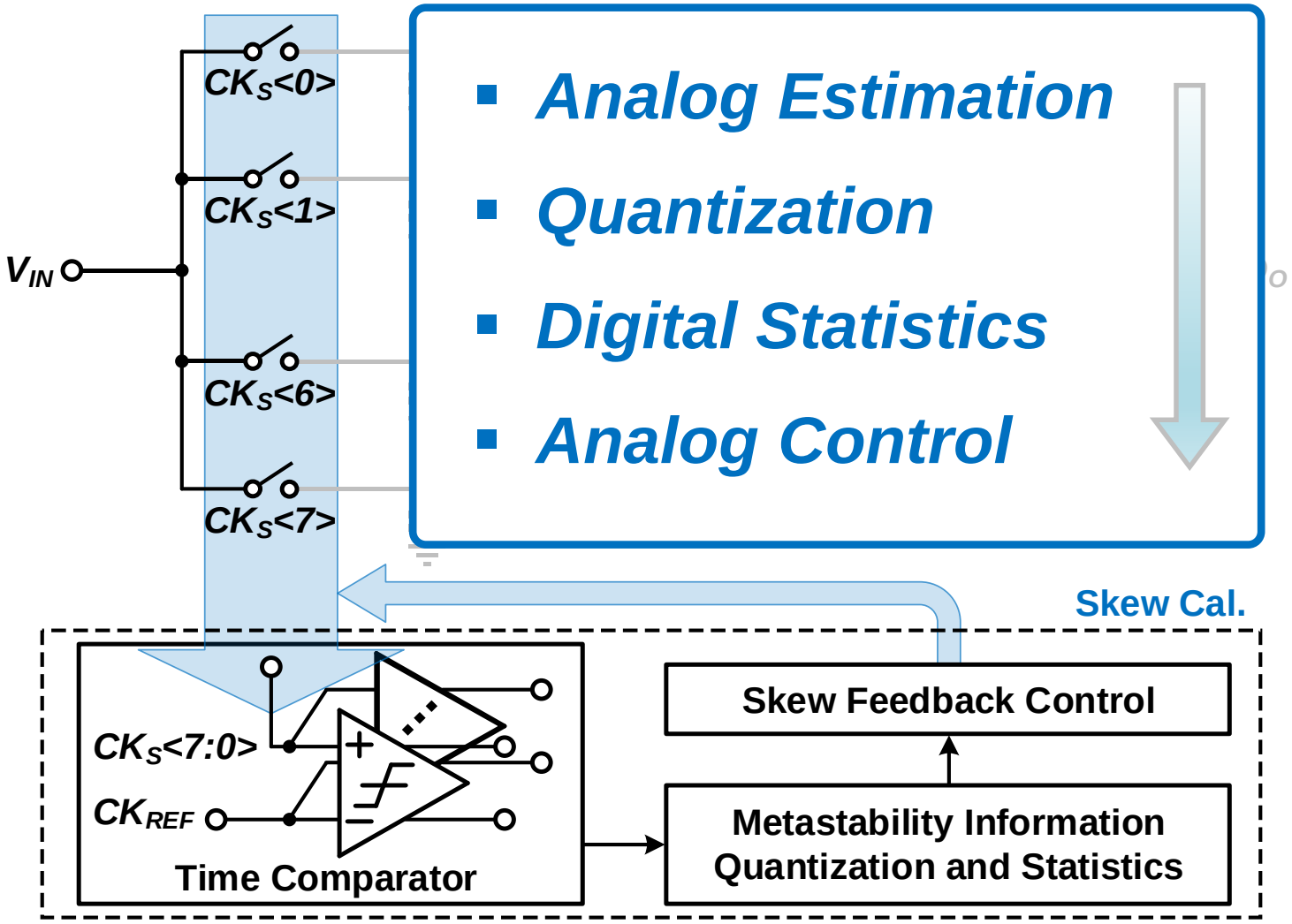
- For <–50dB timing spurs with 10GHz input → **skew(σ)<100fs**

Prior Background Timing Skew Cal.

	N. Le Dortz ISSCC 14	B. Razavi JSSC 13	M. El-Chammas JSSC 11	S. Lee ISSCC 14
Type	All Digital Approach	Digital Estimation and Analog Feedback Control		
Estimation Methods	Derivative-based	Auto Correlation	Cross Correlation	Variance-based
Input Signal Limitation	Wide-Sense-Stationary & $<F_S/2$	Wide-Sense-Stationary	Busy Enough & Crossing Zero	Busy Enough & Large Swing
Extra Hardware	High-Speed Digital Filter	No	1-bit Reference ADC	Full-Speed Flash ADC

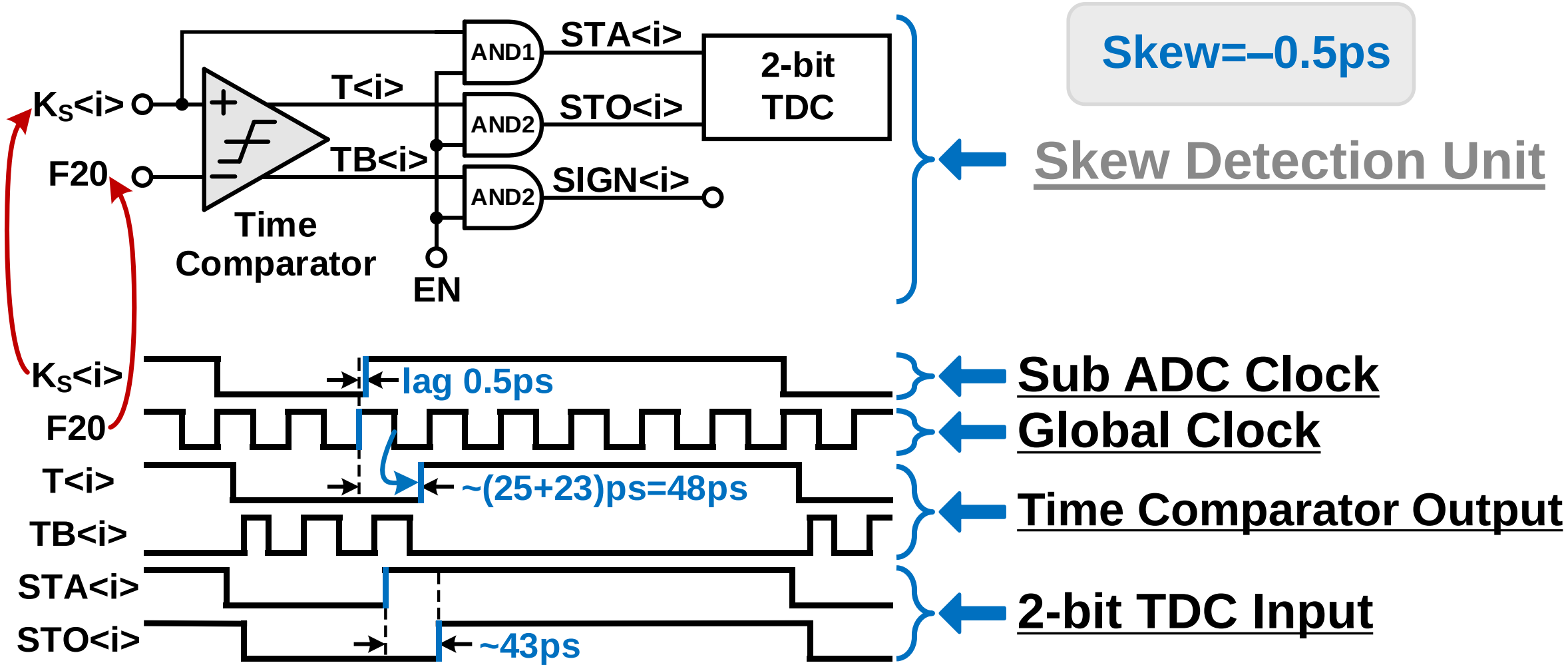
- All rely on certain input conditions

Objectives

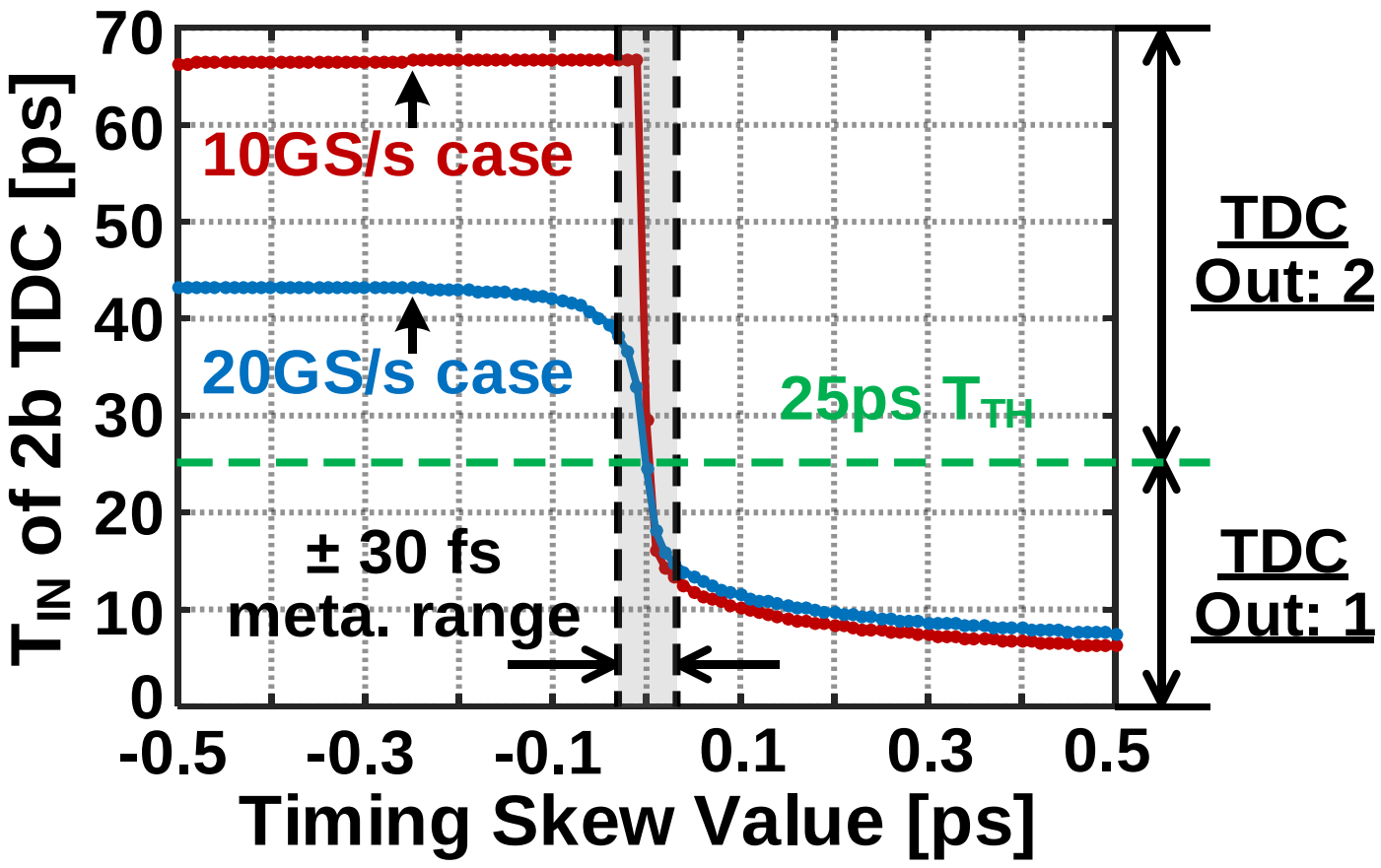


- **Timing Skew Cal.:**
  1. Does not rely on ADC input (background)
  2. Does not base on A/D quantization
  3. Remaining skew(σ) <100fs
  4. Small amount of iterations

Timing Skew Detection – (Skew<0)

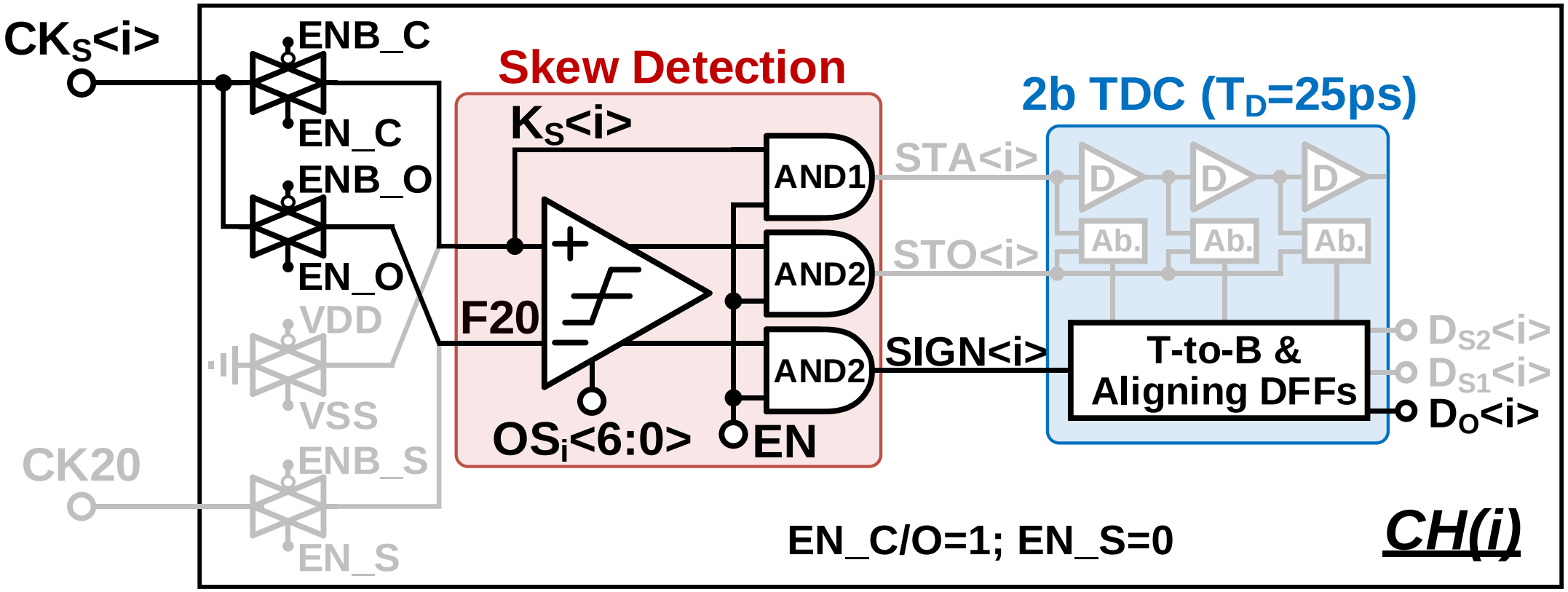


Detection T_{IN} vs. Timing Skew Value



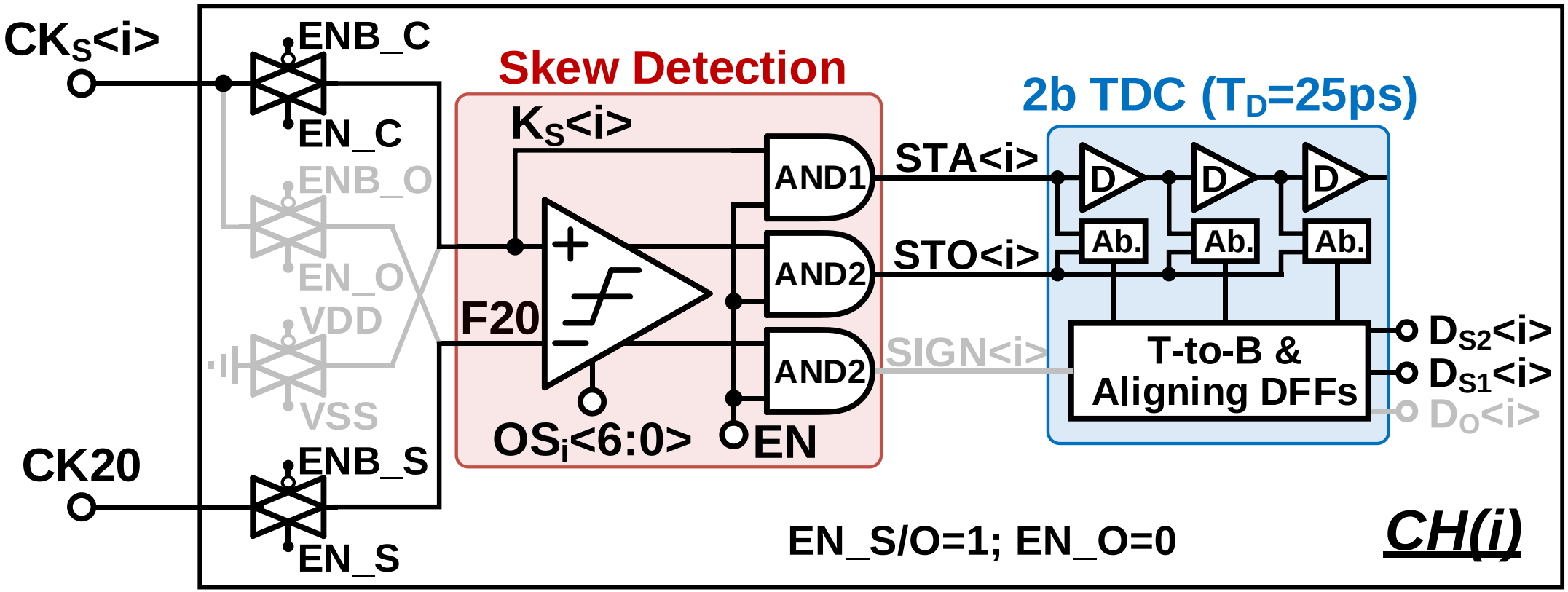
- **Quantization:**
  → 2b TDC (T_{LSB}=25ps)
- **Bound Accuracy:**
  → ±30fs (meta. range)
- **Comparator Noise:**
  → 1k-sample statistics for one decision

Calibration – Time Comparator Offset



- Passive switches + 1k-sample statistics on D_O<i>

Calibration – Time Skew



- Passive switches + 1k-sample statistics on D_{S2}<i> & D_{S1}<i>

Timing Skew Calibration Comparison

	N. Le Dortz ISSCC 14	S. Lee ISSCC 14	B. Razavi JSSC 13	El-Chammas JSSC 11	V. H.-C. Chen ISSCC 14	This Work
Type	All Digital Approach	Digital Estimation and Analog Feedback Control			Analog Estimation and Analog Feedback Control	
Estimation Methods	Derivative-based	Variance-based	Auto Correlation	Cross Correlation	Build-in Cal Signal	Direct Timing Comparison
Unlimited Input Signal	X Wide-Sense-Sta. & <$F_S/2$	X Busy Enough & Large Swing	X Wide-Sense-Stationary	X Busy Enough & Crossing Zero	√	√
Constant Input Impedance	√	√	√	X	X	√
Timing Spur After Cal	–70dB @0.6GHz F_{IN}	–60dB @0.5GHz F_{IN}	–75dB @0.6GHz F_{IN}	–41dB @8.0GHz F_{IN}	–42dB @8.2GHz F_{IN}	–55dB @10GHz F_{IN}

Comparison

	This Work		S. Kim VLSI 20	B. Xu VLSI 16	V.H.-C. Chen ISSCC 14	Y. Frans VLSI 16
Architecture	**TI-Time**		TI-Time	TI-SAR/TDC	TI-Flash	TI-SAR
Technology	**65nm CMOS**		16nm FinFET	28nm CMOS	32nm SOI	16nm FinFET
Area [mm^2]	**0.22**		0.10	0.03	0.25	-
Channel Number	**8×**		16×	16×	8×	32×
Resolution [bits]	**8**		8	6	6	8
Supply [V]	**1.0/1.2***	**0.85/1.05***	0.9	0.85/0.95	0.9	0.9
Sampling [GS/s]	**20**	**16**	20	24	20	28
3dB-BW (GHz)	**>16**	**>16**	-	-	-	-
SNDR LF_{IN} [dB]	**41.0**	**40.2**	35.0	34.8	34.8	40.9
SNDR HF_{IN} [dB]	**38.8**	**38.1**	32.5	28.9	30.7	31.5
HF_{IN} [GHz]	**10.0**	**8.0**	1.0	11.9	10	14.0
Power [mW]	**129.9**	**76.2**	175.2	23.0	69.5	280.0
FoM_{LF} [fJ/conv.-step]	**70.9**	**57.0**	190.5	21.3	77.4	110.4
FoM_{HF} [fJ/conv.-step]	**91.3**	**72.6**	254.0	42.1	124.1	325.7

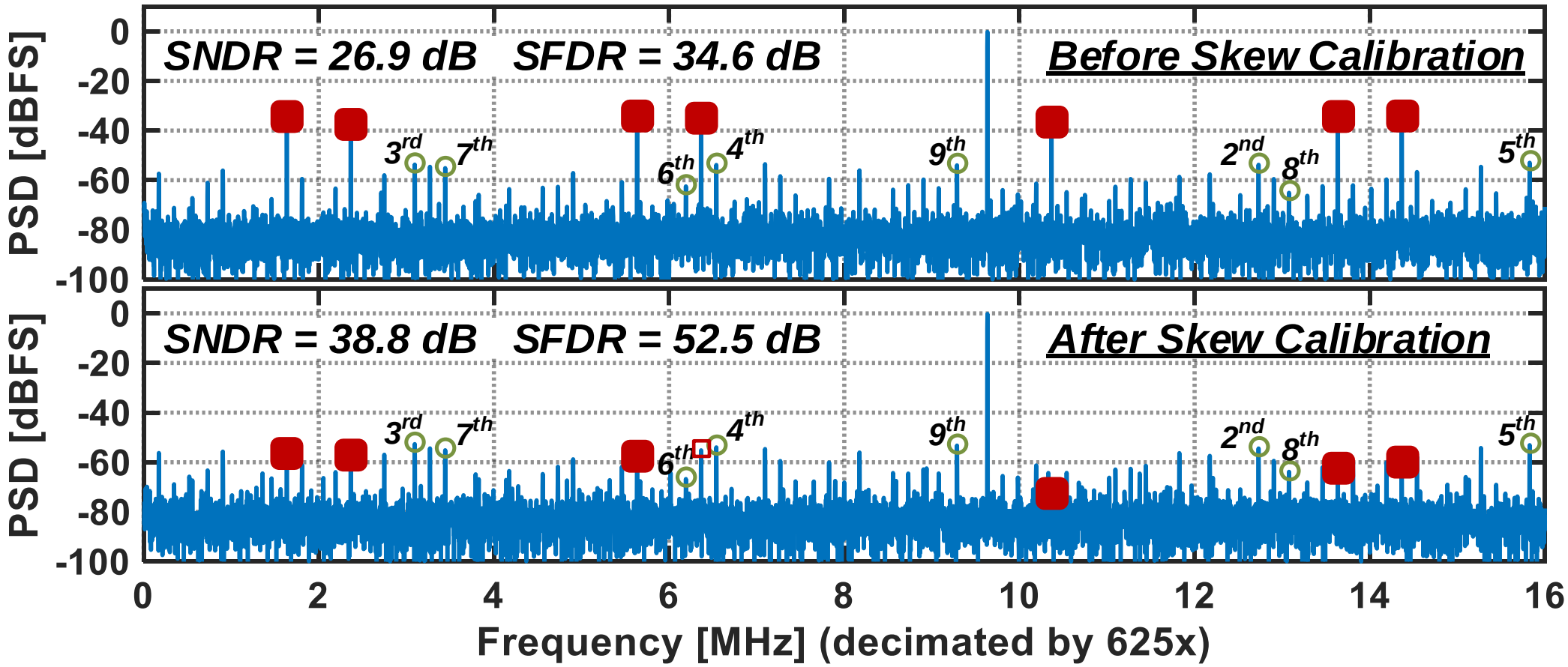
* Timing skew calibration works with a higher supply and 10% activation rate.

Time-Skew Calibration Measurement

- F_{IN} = 9.974365 GHz
- F_S = 20 GS/s

Timing Spurs

Harmonics (2^{nd}-9^{th})

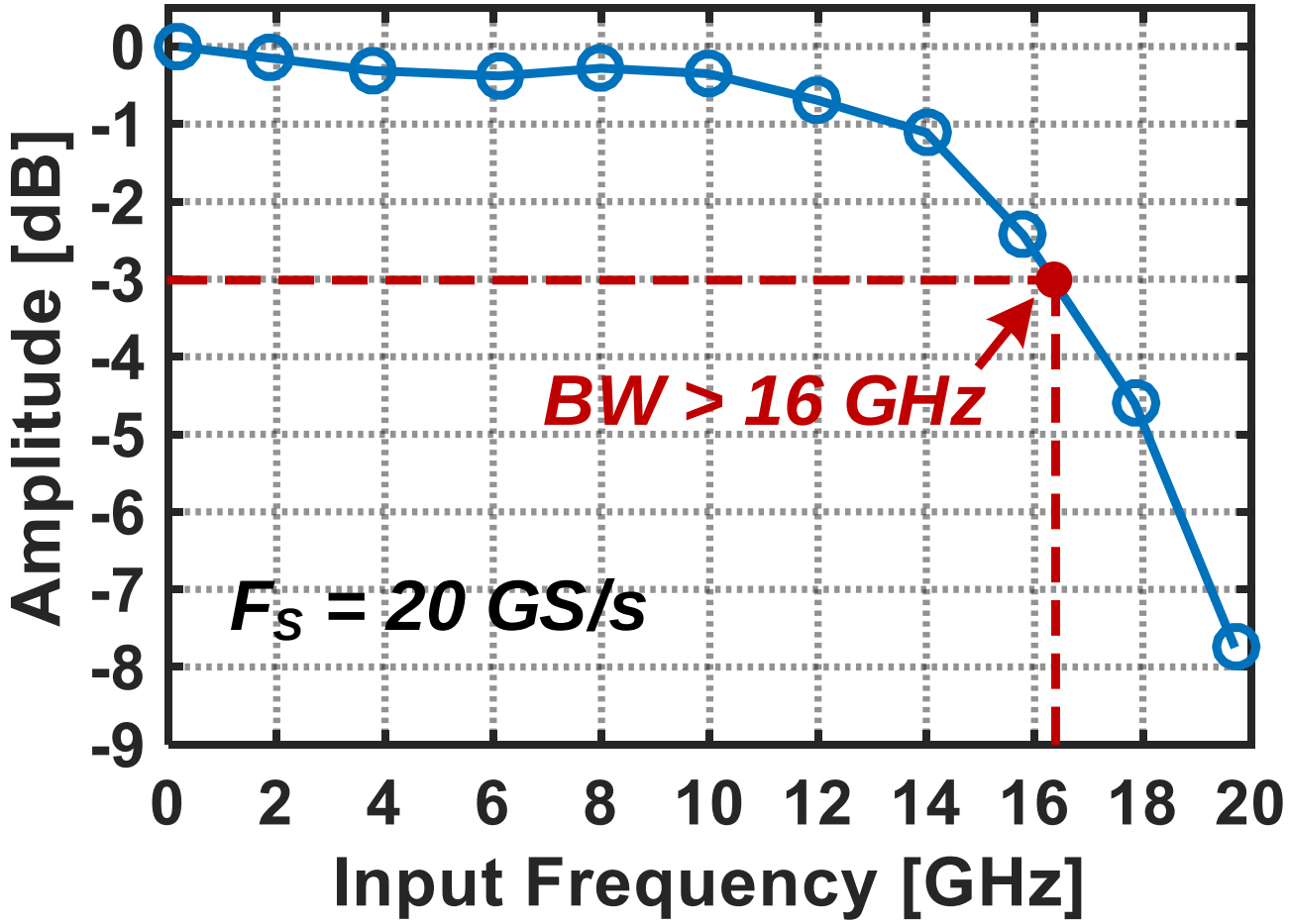


Timing Spurs:

-34.6dB

-55.2dB

Bandwidth Measurement



- Measured with input probe needle
- Benefit from inherent sub-channel buffer and 45-fF C_S

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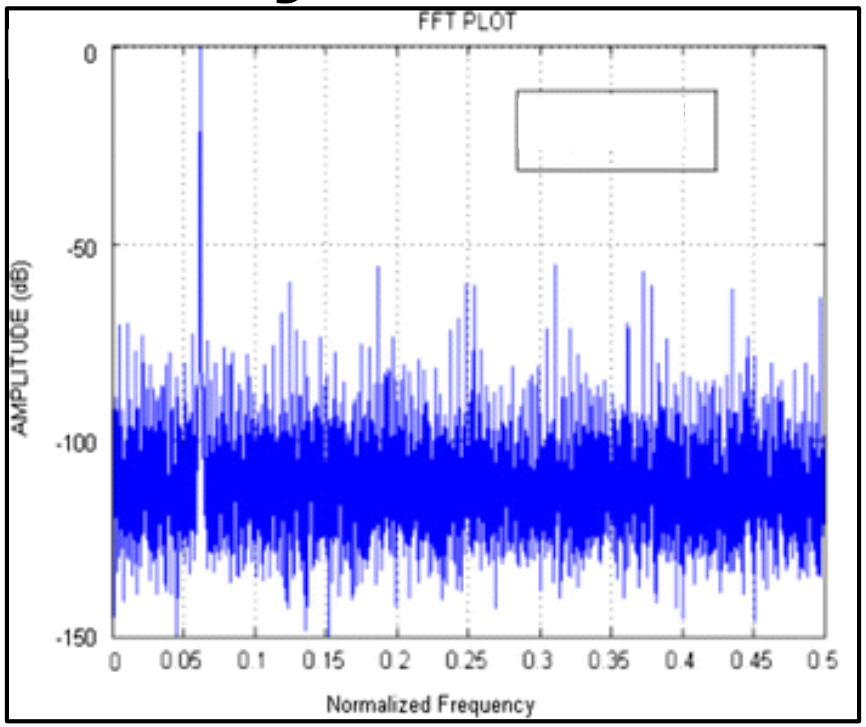
- ❑ **Conclusion**

Future Works and Conclusion

- Many hybrid ADC architectures in recent year, how about calibration?
- Analog-assisted is a good topic
- Utilized concept from AI
- Eventually, things are still fundamental, about … cost

Hope you enjoy the workshop and my talk
Thank you for your Attention - Q&A



Thank you for your Attention
Q&A